# ZETTLER DISPLAYS

# SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

	CUSTOMER APP	ROVAL	
<b>※ PART</b> 1	NO.: <u>ATM0700L61 (ZE</u>	ETTLER DISPLA	AYS) VER1.1
APPROVAL		COMPANY CHOP	
CUSTOMER COMMENTS			

ZETTLER DIS	ZETTLER DISPLAYS ENGINEERING APPROVAL						
DESIGNED BY	CHECKED BY	APPROVED BY					
GAOZC							

## **REVISION RECORD**

REVISION	REVISION DATE	PAGE	CONTENTS
VER1.0	2019-06-06		FIRST ISSUE
VER1.1	2019-07-10	ALL	CHANGE SPEC FORMAT

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## 1. GENERAL SPECIFICATIONS

lte	em	Specification	Remark
1. LC	CD size	7.0 inch(Diagonal)	
2. Dr	river element	a-Si TFT active matrix	
3. Re	esolution	1024x(RGB)x600	
4. Dis	splay mode	IPS, Normally black, Transmissive	
5. Do	ot Pitch (W*H)	0.05mm(W) x 0.15mm(H)	
6. Pi	ixel pitch(W*H)	0.15mm(W) x 0.15mm(H)	
7. Ad	ctive Area(W*H)	154.2mm(W) x 85.92mm(H)	
8. M	lodule size (W*H)	164.9mm(W) x 100.0mm(H) x 3.5mm(D)	Note 1
9. St	urface treatment	Glare	
11. Co	olor arrangement	RGB-stripe	
12. Co	olor	16.7M / 262K	
13. Int	terface	4-lane / 3-lane LVDS interface	
14. W	/eight	T.B.D.	
15. Ro	oHS	RoHS compliant	

Note 1: Please refer to mechanical drawing.

## 2. PIN ASSIGNMENT

#### **TFT LCD Panel Driving Section**

FPC Connector is used for the module electronics interface. The recommended model is HIROSE FH33J-40S-0.5SH(10), MOLEX 0541044031 or compatible.

1	Pin No.	Symbol	Function	Level	Note
NC	1	VCOM	Common voltage	Р	
5         RESET         Global reset pin         I           6         STBYB         Standby mode, normally pulled high STBYB = 1, normal operation         I           7         GND         Ground         P           8         RXIN0-         -LVDS differential data input 0         I           9         RXIN0+         +LVDS differential data input 0         I           10         GND         Ground         P           11         RXIN1-         -LVDS differential data input 1         I           12         RXIN1+         +LVDS differential data input 1         I           13         GND         Ground         P           14         RXIN2-         -LVDS differential data input 2         I           15         RXIN2+         +LVDS differential data input 2         I           16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN-         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3-         +LVDS differ	2~3	VDD	Power voltage, 3.3V typical	Р	
6         STBYB         Standby mode, normally pulled high STBYB = 1, normal operation         I           7         GND         Ground         P           8         RXIN0-         -LVDS differential data input 0         I           9         RXIN0+         +LVDS differential data input 0         I           10         GND         Ground         P           11         RXIN1-         -LVDS differential data input 1         I           12         RXIN1+         +LVDS differential data input 1         I           13         GND         Ground         P           14         RXIN2-         -LVDS differential data input 2         I           15         RXIN2+         +LVDS differential dock input 2         I           16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input I         I           18         RXCLKIN+         +LVDS differential clock input I         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND	4	NC	No connection	-	
6         STBYB         STBYB = 1, normal operation STBYB = 0, display shutdown         I           7         GND         Ground         P           8         RXIN0-         -LVDS differential data input 0         I           9         RXIN0+         +LVDS differential data input 0         I           10         GND         Ground         P           11         RXIN1-         -LVDS differential data input 1         I           12         RXIN1+         +LVDS differential data input 1         I           13         GND         Ground         P           14         RXIN2-         -LVDS differential data input 2         I           15         RXIN2+         +LVDS differential data input 2         I           16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN+         +LVDS differential data input 3         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Grou	5	RESET	Global reset pin	I	
8         RXIN0-         -LVDS differential data input 0         I           9         RXIN0+         +LVDS differential data input 0         I           10         GND         Ground         P           11         RXIN1-         -LVDS differential data input 1         I           12         RXIN1+         +LVDS differential data input 1         I           13         GND         Ground         P           14         RXIN2-         -LVDS differential data input 2         I           15         RXIN2+         +LVDS differential data input 2         I           16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN+         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P	6	STBYB	STBYB = 1 ,normal operation	I	
9         RXIN0+         +LVDS differential data input 0         I           10         GND         Ground         P           11         RXIN1-         -LVDS differential data input 1         I           12         RXIN1+         +LVDS differential data input 1         I           13         GND         Ground         P           14         RXIN2-         -LVDS differential data input 2         I           15         RXIN2+         +LVDS differential data input 2         I           16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN+         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27 </td <td>7</td> <td>GND</td> <td>Ground</td> <td>Р</td> <td></td>	7	GND	Ground	Р	
10	8	RXIN0-	-LVDS differential data input 0	I	
11	9	RXIN0+	+LVDS differential data input 0	I	
12	10	GND	Ground	Р	
13	11	RXIN1-	-LVDS differential data input 1	I	
14         RXIN2-         -LVDS differential data input 2         I           15         RXIN2+         +LVDS differential data input 2         I           16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN+         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           6bit/8bit mode select         LVBIT="L", 6-bit. LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horiz	12	RXIN1+	+LVDS differential data input 1	I	
15	13	GND	Ground	Р	
16         GND         Ground         P           17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN+         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         Gbit/8bit mode select         LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift town:         I           SHLR = "H", shift down:         I	14	RXIN2-	-LVDS differential data input 2	I	
17         RXCLKIN-         -LVDS differential clock input         I           18         RXCLKIN+         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         Gbit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left: SHLR = "H", shift right:         I           Vertical inversion         SHLR = "L", shift down: SHLR = "H", shift up:         I	15	RXIN2+	+LVDS differential data input 2	I	
18         RXCLKIN+         +LVDS differential clock input         I           19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         6bit/8bit mode select LVBIT="L", 6-bit. LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           4         Horizontal inversion         SHLR = "L", shift left: SHLR = "H", shift down: SHLR = "L", shift down: SHLR = "H", shift down: SHLR = "H", shift down:         I           34         U/D         SHLR = "L", shift down: SHLR = "H", shift up:         I	16	GND	Ground	Р	
19         GND         Ground         P           20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         6bit/8bit mode select         I           LVBIT="L", 6-bit. LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           4         Horizontal inversion         SHLR = "L", shift left:         I           5HLR = "H", shift down:         I         SHLR = "L", shift down:         I           5HLR = "H", shift up:         I         SHLR = "H", shift up:	17	RXCLKIN-	-LVDS differential clock input	I	
20         RXIN3-         -LVDS differential data input 3         I           21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         LVBIT="L", 6-bit. LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           4         Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion         I           34         U/D         SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	18	RXCLKIN+	+LVDS differential clock input	I	
21         RXIN3+         +LVDS differential data input 3         I           22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         Gbit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion           SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	19	GND	Ground	Р	
22         GND         Ground         P           23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         Gbit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion SHLR = "L", shift left: SHLR = "H", shift right:         I           Vertical inversion SHLR = "L", shift down: SHLR = "L", shift up:         I	20	RXIN3-	-LVDS differential data input 3	I	
23~24         NC         No connection         -           25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         6bit/8bit mode select LVBIT="L", 6-bit. LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         I           Vertical inversion         SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	21	RXIN3+	+LVDS differential data input 3	I	
25         GND         Ground         P           26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         Gbit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion           SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	22	GND	Ground	Р	
26         NC         No connection         -           27         DIMO         Backlight CABC controller signal         O           28         SELB         6bit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion           34         U/D         SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	23~24	NC	No connection	-	
27         DIMO         Backlight CABC controller signal         O           28         SELB         6bit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion           34         U/D         SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	25	GND	Ground	Р	
27         DIMO         Backlight CABC controller signal         O           28         SELB         6bit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion           34         U/D         SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	26	NC	No connection	-	
28         SELB         6bit/8bit mode select LVBIT="H", 8-bit.         I           29         AVDD         Power for analog circuit         P           30         GND         Ground         P           31~32         LED-         LED cathode         P           Horizontal inversion         SHLR = "L", shift left:         I           SHLR = "H", shift right:         Vertical inversion           34         U/D         SHLR = "L", shift down:         I           SHLR = "H", shift up:         I	27	DIMO	Backlight CABC controller signal	0	
30   GND   Ground   P			6bit/8bit mode select	_	
31~32 LED- LED cathode P  Horizontal inversion  SHLR = "L", shift left:  SHLR = "H", shift right:  Vertical inversion  SHLR = "L", shift down:  SHLR = "H", shift up:	29	AVDD	Power for analog circuit	Р	
Horizontal inversion  SHLR = "L", shift left:  SHLR = "H", shift right:  Vertical inversion  SHLR = "L", shift down:  SHLR = "H", shift up:	30	GND	Ground	Р	
33 L/R SHLR = "L", shift left:  SHLR = "H", shift right:  Vertical inversion  SHLR = "L", shift down:  SHLR = "H", shift up:	31~32	LED-	LED cathode	Р	
34 U/D SHLR = "L", shift down:   SHLR = "H", shift up:			Horizontal inversion SHLR = "L", shift left:	ı	
25 VCI Cote off college	34	U/D	SHLR = "L", shift down:	I	
אס ן vGL ן Gale off voltage   P	35	VGL	Gate off voltage	Р	

36~37	GND	Ground	Р	
38	VGH	Gate on voltage	Р	
39~40	LED+	LED anode	Р	

I: input, O: output, P: Power

## 3. Operating Specification

#### 3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Val	ues	Unit	Remark
item	Symbol	Min. Max.		Oilit	Kemark
	$V_{DD}$	-0.5	3.96	V	
Power Voltage	$AV_DD$	-0.5	14.85	V	
Power Voltage	$V_{GH}$	-0.3	42	V	
	V <sub>GL</sub>	-42	0.3	V	
Operation Temperature	T <sub>OP</sub>	-20	70	°C	
Storage Temperature	T <sub>ST</sub>	-30	80	°C	
LED Reverse Voltage	V <sub>R</sub>	-	1.2	V	Each LED Note 2
LED Forward Current	I <sub>F</sub>		25	mA	Each LED

**Note 1**: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

Note 2: V<sub>R</sub> Conditions: Zener Diode 20mA

#### 3.1.1 Typical Operation Conditions

Item	Symbol		Values	Unit	Remark	
item	Symbol	Min.	Тур.	Max.	Oilit	Keiliaik
	$V_{DD}$	3.0	3.3	3.6	V	
Power Voltage	$AV_DD$	9.4	9.6	9.8	V	
Power voitage	$V_{GH}$	17.5	18.0	18.5	V	
	$V_{GL}$	-6.5	-6	-5.5	V	
Input Signal Voltage	$V_{COM}$	2.3	3.5	4.2	V	
Input Logic High Voltage	V <sub>IH</sub>	$0.7DV_{DD}$		$DV_{DD}$	V	
Input Logic Low Voltage	V <sub>IL</sub>	0		$0.3DV_{DD}$	V	

**Note 1**: Be sure to apply  $V_{DD}$  and  $V_{GL}$  to the LCD first, and then apply  $V_{GH}$ .

#### 3.1.2 Current Consumption

Item	Symbol	\	/alues	Unit	Remark		
item	Symbol	Min.	Тур.	Max.	Oilit	Nemark	
	I <sub>GH</sub>		5.2	10.2	mA	V <sub>GH</sub> =18.0V	
Power Voltage	I <sub>GL</sub>		4.7	9.7	mA	V <sub>GL</sub> =-6.0V	
Power Voltage	I <sub>VDD</sub>		14	19	mA	V <sub>DD</sub> =3.3V	
	I <sub>AVDD</sub>		31.0	50.0	mA	AV <sub>DD</sub> =9.6V	

## 3.1.3 Backlight driving conditions

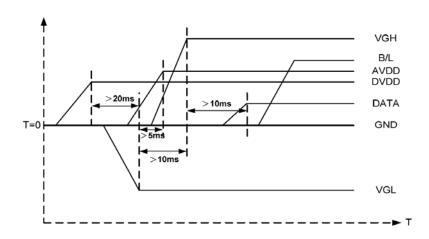
ltem	Symbol		Values	Unit	Remark		
item	Symbol	Min.	Тур.	Max.	Oilit	Remark	
Voltage for LED Backlight	V <sub>L</sub>	9.0	9.9	10.5	V	Note 1	
Current for LED Backlight	ΙL	-	180	-	mA		
LED life time		30000			Hr	Note 2	

**Note 1**: The LED Supply Voltage is defined by the number of LED at Ta=25 $^{\circ}$ C and I<sub>L</sub> =180mA.

**Note 2**: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25  $^{\circ}$ C and I<sub>L</sub> =180mA.

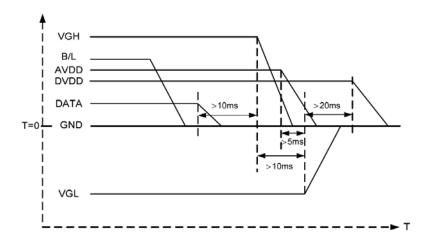
#### 3.2 Power Sequence

#### a.Power on:



$$V_{DD} {\rightarrow} V_{GL} {\rightarrow} V_{GH} {\rightarrow} Data {\rightarrow} B/L$$

#### b.Power off:

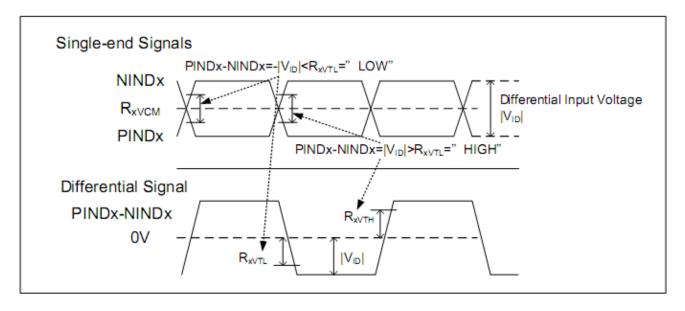


$$B/L \rightarrow Data \rightarrow V_{GH} \rightarrow V_{GL} \rightarrow V_{DD}$$

## 3.3 Timing Characteristics

#### 3.3.1 DC Electrical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Únit	Condition
Differential input high threshold voltage	$R_{xVTH}$	0.1	0.2	0.3	>	- R <sub>xVCM</sub> = 1.2V
Differential input low threshold voltage	R <sub>xVTL</sub>	-0.3	-0.2	-0.1	>	N <sub>X</sub> VCM = 1.2 V
Input voltage range (singled-end)	R <sub>XVIN</sub>	0.7	•	1.7	٧	
Differential Input Impedance	Z <sub>ID</sub>	80	100	125	ohm	
Differential input common mode voltage	R <sub>xVCM</sub>	1	1.2	1.4	٧	V <sub>ID</sub>  =0.2V
Differential input voltage	V <sub>ID</sub>	0.2	•	0.6	٧	
Differential input leakage current	I <sub>LCLVDS</sub>	-10	1	+10	uA	
LVDS Digital Operating Current	I <sub>VDDLVDS</sub>	•	TBD	TBD	mA	F <sub>CLK</sub> =52 MHz, frame rate 60Hz, VDD=3.3V.
LVDS Digital Stand-by Current	I <sub>STLVDS</sub>	1	TBD	TBD	uA	Clock & all Functions are stopped.



## **3.3.2 Timing**

# DE mode

DE mode					
Parameter	Symbol		Unit		
Falanietei	Symbol	Min.	Тур.	Max.	Offic
DCLK frequency @Frame rate=60hz	fclk	40.8	51.2	67.2	Mhz
Horizontal display area	thd	1024			DCLK
HSYNC period time	th	1114	1344	1400	DCLK
HSYNC blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd	600		Н	
VSYNC period time	tv	610	635	800	Н
VSYNC blanking	tvb+tvfp	10	35	200	Н

#### HV mode(1)

HV mode
---------

Horizontal input timing

Danier Combal Value									
Parameter		Symbol	Value			Unit			
Horizontal display a	area	thd		1024					
DCLK fraguanav@ Frama	fclk	Min.	Тур.	Max.					
DCLK frequency@ Frame	ICIK	44.9	51.2	63	Mhz				
1 Horizontal Line	9	th	1200	1344	1400				
	Min.		1						
HSYNC pulse width	Тур.	thpw		_		DCLK			
Max.				140		DOLK			
HSYNC back por	thbp	160	160	160					
HSYNC front por	thfp	16	160	216	1				

## HV mode(2)

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	v	<b>CI</b>	uca		ull		mu

Parameter	Cymphol		Unit		
Parameter	Symbol	Min.	Тур.	Max.	Unit
Vertical display area	tvd		600	•	Н
VSYNC period time	tv	624	635	750	Н
VSYNC pulse width	tvpw	1	_	20	Н
VSYNC back porch	tvb	23	23	23	Н
VSYNC front porch	tvfp	1	12	127	Н

## **4.0 OPTICAL SPECIFICATIONS**

Item	Symbol	Condition		Values		Unit	Remark
item	Syllibol	Condition	Min.	Тур.	Max.	Oille	Keillaik
	$\theta_{L}$	Φ=180°(9 O'CLOCK)	70	80			Note 1
Viewing Angle	$\theta_{R}$	Φ=0°(3 O'CLOCK)	70	80		degree	
(CR≥10)	$\theta_{T}$	Φ=90°(12 O'CLOCK)	70	80			
	$\theta_{B}$	Φ=270°(6 O'CLOCK)	70	80			
Response Time $T_{\text{OFF}}$				30		msec	Note 3
Contrast Ratio	CR		600	800			Note 4
	W <sub>x</sub>	Normal	0.26	0.31	0.36		Note 2
Color Chromaticity		Θ=Ф=0°					Note 5
	$W_{Y}$		0.28	0.33	0.38		Note 6
Luminance	L		500	600		cd/m <sup>2</sup>	Note 6
Luminance Uniformity	YU		75	80		%	Note 7

#### **Test Conditions:**

- 1. IL=180mA (Backlight current), the ambient temperature is 25℃.
- 2. The test systems refer to Note 2.

#### Note 1: Definition of viewing angle range

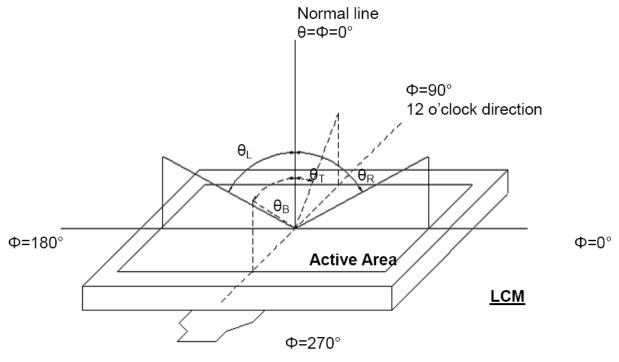


Figure 4.1 Definition of viewing angle.

#### Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON

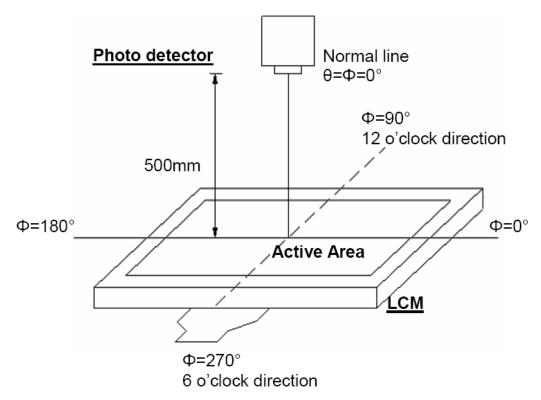


Figure 4.2 Optical measurement system setup

#### Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

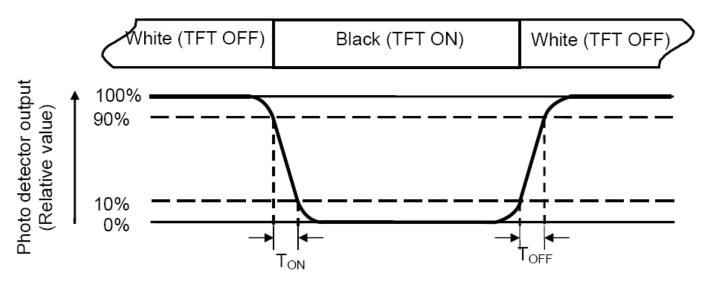


Figure 4.3 Definition of response.

#### Note 4: Definition of contrast ratio

 $\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD on the "white" state}}{\text{Luminance measured when LCD on the "black" state}}$ 

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4 ). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (Yu) = 
$$\frac{B_{min}}{B_{max}}$$

L-----Active area length W----- Active area width

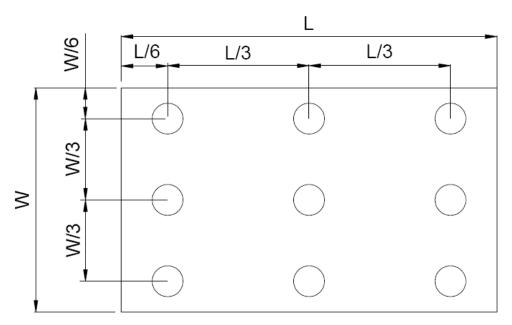


Figure 4.3 Definition of measuring points.

Bmax: The measured maximum luminance of all measurement position. Bmin: The measured minimum luminance of all measurement position.

## **5. RELIABILITY TEST**

Item	Test Condition Item	Remark
High temperature storage	Ta= 80 °C 96hrs	Note 1 Note 3
Low temperature storage	Ta=-30 °C 96hrs	Note 1 Note 3
High temperature operation	Ts= 70 °C 96hrs	Note 2 Note 3
Low temperature operation	Ts=-20 °C 96hrs	Note 1 Note 3
High temperature/High humidity operation	90% RH 60°C 96hrs	Note 3
Thermal Shock	-30℃/30 min ~ +80℃/30 min for a total 10 cycles, Start with cold temperature and end with high temperature.	Note 3
Vibration test	Freq:10~55~10Hz Amplitude:1.5mm 30 minutes for each direction of X,Y,Z	
Package drop test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro static discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

**Note 1**: Ta is the ambient temperature of samples.

**Note 2**: Ts is the temperature of panel's surface.

**Note 3**: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

#### 6. PRECAUTION FOR USING LCM

- When design the product with this LCD Module, make sure the viewing angle matches to its purpose of usage.
- 2. As LCD panel is made of glass substrate, Dropping the LCD module or banging it against hard objects may cause cracking or fragmentation. Especially at corners and edges.
- 3. Although the polarizer of this LCD Module has the anti-glare coating, always be careful not to scratch its surface. Use of a plastic cover is recommended to protect the surface of polarizer.
- 4. If the LCD module is stored at below specified temperature, the LC material may freeze and be deteriorated. If it is stored at above specified temperature, the molecular orientation of the LC material may change to Liquid state and it may not revert to its original state. Excessive temperature and humidity could cause polarizer peel off or bubble. Therefore, the LCD module should always be stored within specified temperature range.
- 5. Saliva or water droplets must be wiped off immediately as those may leave stains or cause color changes if remained for a long time. Water vapor will cause corrosion of ITO electrodes.
- 6. If the surface of LCD panel needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If it is not still clean enough, blow a breath on the surface and wipe again.
- 7. The module should be driven according to the specified ratings to avoid malfunction and permanent damage. Applying DC voltage cause a rapid deterioration of LC material. Make sure to apply alternating waveform by continuous application of the M signal. Especially the power ON/OFF sequence should be kept to avoid latch-up of driver LSIs and DC charge up to LCD panel.
- 8. Mechanical Considerations
  - a) LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
  - b) Do not tamper in any way with the tabs on the metal frame.
  - c) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
- 9. Static Electricity
  - a) Operator

Wear the electrostatics shielded clothes because human body may be statically charged if not ware shielded clothes. Never touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.

b) Equipment

There is a possibility that the static electricity is charged to the equipment, which has a function of peeling or friction action (ex: conveyer, soldering iron, working table). Earth the equipment through proper resistance (electrostatic earth: 1x10<sup>8</sup> ohm).

Only properly grounded soldering irons should be used.

If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.

The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

c) Floor

Floor is the important part to drain static electricity, which is generated by operators or equipment.

There is a possibility that charged static electricity is not properly drained in case of insulating floor. Set the electrostatic earth (electrostatic earth: 1x10<sup>8</sup> ohm).

d) Humidity

Proper humidity helps in reducing the chance of generating electrostatic charges. Humidity should be kept over 50%RH.

e) Transportation/storage

The storage materials also need to be anti-static treated because there is a possibility that the human body or storage materials such as containers may be statically charged by friction or peeling.

The modules should be kept in antistatic bags or other containers resistant to static for storage.

f) Soldering

Soldering anything to this TFT display would void the warranty.

g) Others

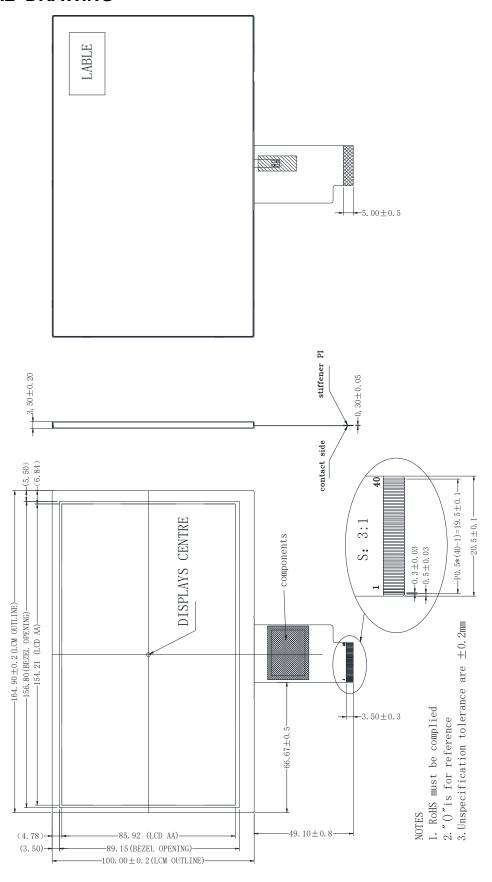
The laminator (protective film) is attached on the surface of LCD panel to prevent it from scratches or stains. It should be peeled off slowly using static eliminator.

Static eliminator should also be installed to the workbench to prevent LCD module from static charge.

- 10. Operation
  - a) Driving voltage should be kept within specified range; excess voltage shortens display life.
  - b) Response time increases with decrease in temperature.
  - c) Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear "fractured".
  - d) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

- 11. If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. The toxicity is extremely low but caution should be exercised at all the time.
- 12. Disassembling the LCD module can cause permanent damage and it should be strictly avoided.
- 13. LCD retains the display pattern when it is applied for long time (Image retention). To prevent image retention, do not apply the fixed pattern for a long time. Image retention is not a deterioration of LCD. It will be removed after display pattern is changed.
- 14. Do not use any materials, which emit gas from epoxy resin (hardener for amine) and silicone adhesive agent (dealcohol or deoxym) to prevent discoloration of polarizer due to gas.
- 15. Avoid the exposure of the module to the direct sunlight or strong ultraviolet light for a long time.

## 7. MECHANICAL DRAWING



# 8. PACKAGE DRAWING T.B.D.

#### 9. INSPECTION SPECIFICATION

#### 1. SCOPE SPECIFICATIONS CONTAIN

- 1.1 DISPLAY QUALITY EVALUATION
- 1.2 MECHANICS SPECIFICATION

#### 2. SAMPLING PLAN

UNLESS THERE IS OTHER AGREEMENT, THE SAMPLING PLAN FOR INCOMING INSPECTION SHALL FOLLOW MIL-STD-105E.

- 2.1 LOT SIZE: QUANTITY PER SHIPMENT AS ONE LOT (DIFFERENT MODEL AS DIFFERENT LOT ).
- 2.2 SAMPLING TYPE: NORMAL INSPECTION, SINGLE SAMPLING.
- 2.3 SAMPLING LEVEL: LEVEL II.
- 2.4 AQL: ACCEPTABLE QUALITY LEVEL

MAJOR DEFECT: AQL=0.65 MINOR DEFECT: AQL=1.0

#### 3. PANEL INSPECTION CONDITION

3.1 ENVIRONMENT:

ROOM TEMPERATURE: 25±5°C.

HUMIDITY: 65±5% RH.

ILLUMINATION: 300 ~ 700 LUX.

3.2 INSPECTION DISTANCE:

35±5 CM

3.3 INSPECTION ANGLE:

THE VISION OF INSPECTOR SHOULD BE PERPENDICULAR TO THE SURFACE OF THE MODULE.

3.4 INSPECTION TIME:

PERCEPTIBILITY TEST TIME: 20 SECONDS MAX.

#### 4. DISPLAY QUALITY

4.1 FUNCTION RELATED:

THE FUNCTION DEFECTS OF LINE DEFECT, ABNORMAL DISPLAY, AND NO DISPLAY ARE CONSIDERED MAJOR DEFECTS.

4.2 BRIGHT/DARK DOTS:

Defect Type	Specification	Major	Minor
Bright Dots	N≤ 2		•
Dark Dots	N≤ 3		•
Total Bright and Dark Dots	N≤ 4		•

Note: 1:

The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

The bright dot defect must be visible through 2% ND filter

Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.

#### 4.3 Pixel Definition:

R	G	В	R	G	В	R	G	В	Dot Defect
R	O	В	R	O	В	R	G	В	Adjacent Dot Defect
R	G	m	R	G	В	R	G	В	Cluster

#### Note 1:

If pixel or partial sub-pixel defects exceed 50% of the affected pixel or sub-pixel area, it shall be considered as1 defect.

#### Note 2:

There should be no distinct non-uniformity visible through 2% ND Filter within 2 sec inspection times.

#### 4.4Visual Inspection specifications:

Defect	Туре	Specification Size	Count(N)	Major	Minor
Dot Shape		D ≤0.25 mm	Ignored		
	Scratch and Bubbles in	0.25mm < D ≤ 0.5mm	N ≤ 3		
display area					•
display disc	•/ • D	D > 0.5mm	N=0		
	<u>.</u> ₹				
Navidan Di	no (Only for Toyah nanal)	D≤70mm	N≤4		_
Newton Ri	ng (Only for Touch panel)	D>70mm	N=0		•
TSD Eich E	uos (Only for Touch panel)	0.1mm <d≤0.2mm< td=""><td>N≤4</td><td></td><td></td></d≤0.2mm<>	N≤4		
15P FISH E	yes (Only for Touch panel)	0.2mm <d≤0.3mm< td=""><td>N≤3</td><td></td><td>•</td></d≤0.3mm<>	N≤3		•
(Bubble/Der	nt)	0.3 <d≤0.4< td=""><td>N≤2</td><td></td><td></td></d≤0.4<>	N≤2		
Line Shape		W ≤ 0.01 mm	Ignored		
·	Scratch · Lint and Bubbles	0.01mm< W ≤ 0.05mm	N ≤ 3		
in display a		and L ≤ 3mm	IN ≤ 3		•
		W > 0.05mm or L > 3 mm	N=0		
Bubble in ce	ell (active area)	It should be found by eyes		•	
	Scratch			•	
Bezel	Dirt	No harm		•	
	Wrap	No harm		•	
	Sunken	No harm		•	
	No label			•	
	Inverted label	No		•	
	Broken			•	
1 -11	Dirt	Word can be read.			•
Label	Not clear				•
	Word out of shape	No			•
	Mistake	No		•	
	Position	Be attached on right positio		•	
0	Not enough	No .			•
Screw	Limp	No		•	

Connector	Connection status	No bend on pins and damage	•
FPC/FFC	Broken	No	•

Note: Extraneous substance and scratch not affecting the display of image, for instance, extraneous substance under polarizer film but outside the display area, or scratch on metal bezel and backlight module or polarizer film outside the display area, shall not be considered as defective or non-conforming.